Hall Ticket Number:

Code No.: 6203M

VASAVI COLLEGE OF ENGINEERING *(Autonomous)*, HYDERABAD
M.E. I Year (ECE) II-Semester (Make Up) Examinations, Sept./Oct.- 2015
(Embedded Systems and VLSI Design)

VLSI Physical Design

Time: **3** hours Max. Marks: **70**

*Note: Answer **ALL** questions in **Part-A** and any **FIVE** questions from **Part-B***

Part-A (10 X 2=20 Marks)

1. Draw the structure of vertical BJT.
2. List the various layers involved in the structure of MOSFET.
3. Identify the various methods to prevent latch up.
4. Bring out the importance of via.
5. Draw the stick diagram of a two input NAND gate.
6. Write any two design rules in IC fabrication.
7. Draw the layout of a two input NOR gate.
8. Classify the types of routings that are possible in a VLSI Chip design.
9. Describe the CAD tools used to extract parasitics.
10. Point out the significance of Design Rule Check.

Part-B (5 X 10=50 Marks)

11. a) Explain how resistors and capacitors are generated in ICs? [6]
    b) Describe the physical design flow in VLSI Design. [4]

12. a) Draw the layout of a capacitor. Explain how the capacitor layers are connected to metal? [3]
    b) Explain with an example the technique used to avoid mismatch between devices in analog Integrated circuits. [7]

13. a) List out the various fabrication errors. Explain the effect of alignment inaccuracies on the performance of the IC. [4]
    b) State the advantages of scalable design rules. [6]

14. a) With neat diagrams explain how clock signal is distributed in the chip? [5]
    b) Explain the design hierarchies with an example. [5]

15. a) Distinguish between schematic editor and layout editor. [5]
    b) Give an overview of CAD tools for front end and back end VLSI design. [5]

16. a) Explain about hierarchical stick diagrams with an example. [4]
    b) Draw the CMOS circuit and layout for the following Boolean expression. [6]

$$f = \overline{a + b.c}$$

17. Write short notes on any **two** of the following:
    a) Wienberger Image array [5]
    b) Floor Planning [5]
    c) Cost and Performance analysis [5]

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